iT4134D
X2, 4-to-7 GHz Clock Multiplier
(Advanced Information)

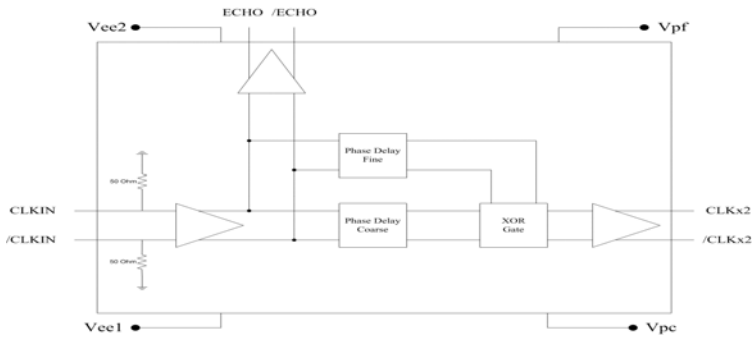
Description

The iT4134D is a high-speed X2 clock multiplier fabricated using 1-µm HBT GaAs technology and employs an ECL topology to guarantee high-speed operation. It is an excellent choice for digital clock multiplication, instrumentation, and edge detection. Digital clock multiplication is implemented via XOR operation between the input clock and an internal delayed replica. Several embedded electrically-controlled phase delays are also employed. Suitable regulation of the phase delay voltage controls allows duty cycle control on the clock outputs. Suitable power supply internal distribution provides the ability to disable the echo input which reduces power consumption. The iT4134D can also be stimulated via NRZ data to perform edge detection. A dedicated temperature monitoring pin is also provided.

Features

- Clock input range: 4 to 7 GHz
- 900 mVpp typical single-ended output
- Input sensitivity: Single-ended input >200 mV
- Jitter RMS <1 ps
- 50-ohm matched inputs and outputs (DC)
- Compatible SCFL I/O levels
- Differential or single-ended I/O
- Duty cycle control
- Echo inputs available
- Power consumption: 1.25 W

Device Diagram



Absolute Maximum Ratings

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameters/conditions	Min.	Max.	Units
V_{EE}	Power supply voltage	-5.5	0	V
VPc	Phase delay voltage control (coarse duty cycle adjustment)	-3.5	0	V
VPf	Phase delay voltage control (fine duty cycle adjustment)	-3.5	0	V
V_{IH}	Data/clock input voltage level, high level	-1.2	1.2	V
V_{IL}	Data/clock input voltage level, low level	-1.2	1.2	V
T_A	Operating temperature range	-15	125	°C
T_{STG}	Storage temperature	-65	150	°C

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Recommended Operating Conditions

Symbol	Parameters/Conditions	Min.	Typ.	Max	Units
Ta	Operating temperature range	0		85	°C
Vee	Power supply voltage		-5		V
Vih	Data/clock input voltage level, high level (single ended)		0.25		V
Vil	Data/clock input voltage level, low level (single ended)		-0.25		V
Vindc	DC input voltage (with DC-coupled input)		0		V

Electrical Characteristics

Symbol	Parameters	Min	Typ	Max	Units
Vee	Power supply voltage	-5.25	-5.0	-4.75	V
Vih	Data/clock input voltage level, high level (single ended)	-0.5	0.25	0.5	V
Vil	Data/clock input voltage level, low level (single ended)	-1	-0.25	0	V
Vindc	DC input voltage (with DC-coupled input) (2)	-0.75	0	0.25	V
VPmon	Internally generated reference voltage for 0 ps delay offset of the embedded phase delays (coarse and fine). (3)	-2.8	-2.6	-2.4	V
VPc	Phase delay voltage control (coarse duty cycle adjustment)	VPmon-0.4		VPmon+0.4	V
VPf	Phase delay voltage control (fine duty cycle adjustment)	VPmon-0.4		VPmon+0.4	V
Voh	Data/clock output voltage level, high level (single ended)	-0.1	0	0	V
Vol	Data/clock output voltage level, low level (single ended)	-1.0	-0.9	0.8	V
Tdc	Duty cycle control	40	50	60	%
RLin	Input return loss (up to 25 GHz)		15		dB
RLout	Output return loss (up to 25 GHz)		6		dB
Fclk	Input clock frequency	3.0		7.0	GHz
Jpp	Peak to peak jitter	4	5	6	ps
Jrms	RMS jitter	0.7	0.9	1	ps
SHS	Sub-harmonic suppression	15	20	25	mA
Ic	Power supply current (4)	235	250	280	mA
Pd	Power dissipation (4)	1.1	1.25	1.5	W

1. Electrical characteristics at ambient temperature.
2. In case of single-ended inputs the unused pin has to be tied to VINDC. In case of single-ended output the unused one has to be terminated via 50 ohms to ground.
3. The pin VPmon can be left open or sensed with high-impedance load for temperature monitoring.
4. In case of echo inputs, an extra 65-mA (325-mW) at -5 V must be taken into account

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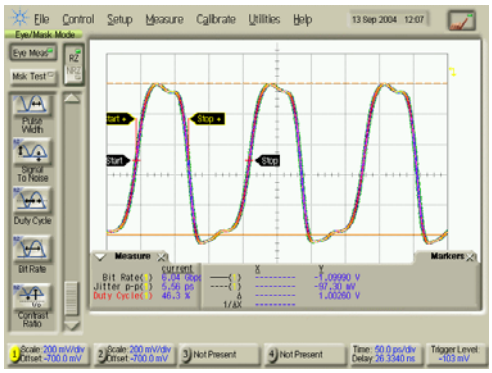
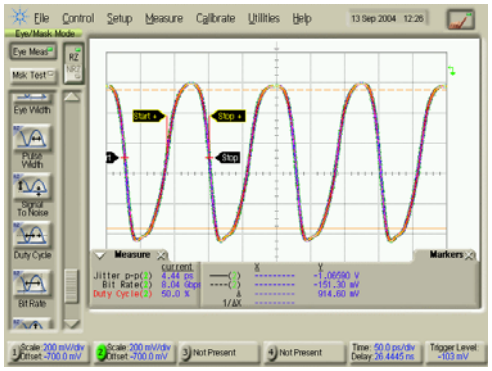
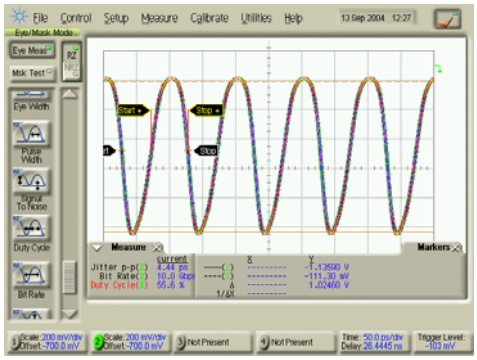
Eye Diagram Performance



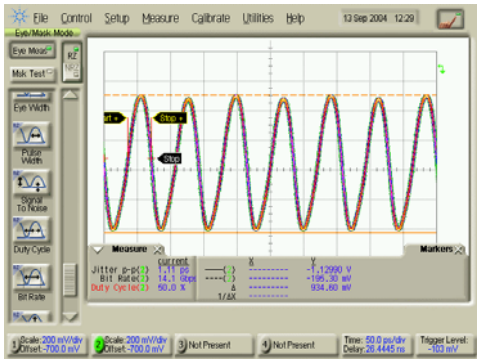
Die measurement
Vee: -5.0 V
Clock input frequency: 3.0 GHz
Single-ended clock input: +/-250 mVpp



Die measurement
Vee: -5.0 V
Clock input frequency: 4.0 GHz
Single-ended clock input: +/-250 mVpp

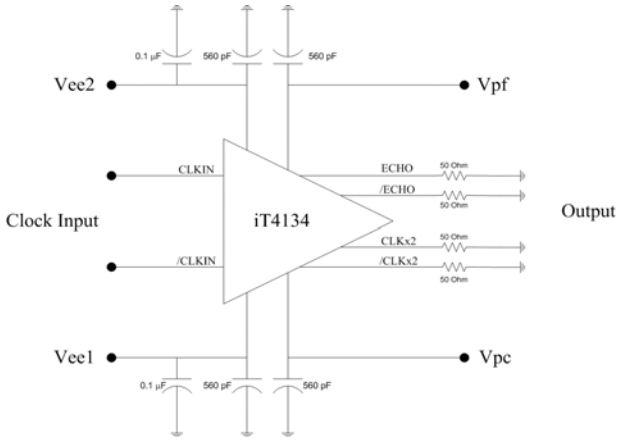


Die measurement
Vee: -5.0 V
Clock input frequency: 5.0 GHz
Single-ended clock input: +/-250 mVpp



Die measurement
Vee: -5.0 V
Clock input frequency: 7.0 GHz
Single-ended clock input: +/-250 mVpp

Recommended Operational Setup



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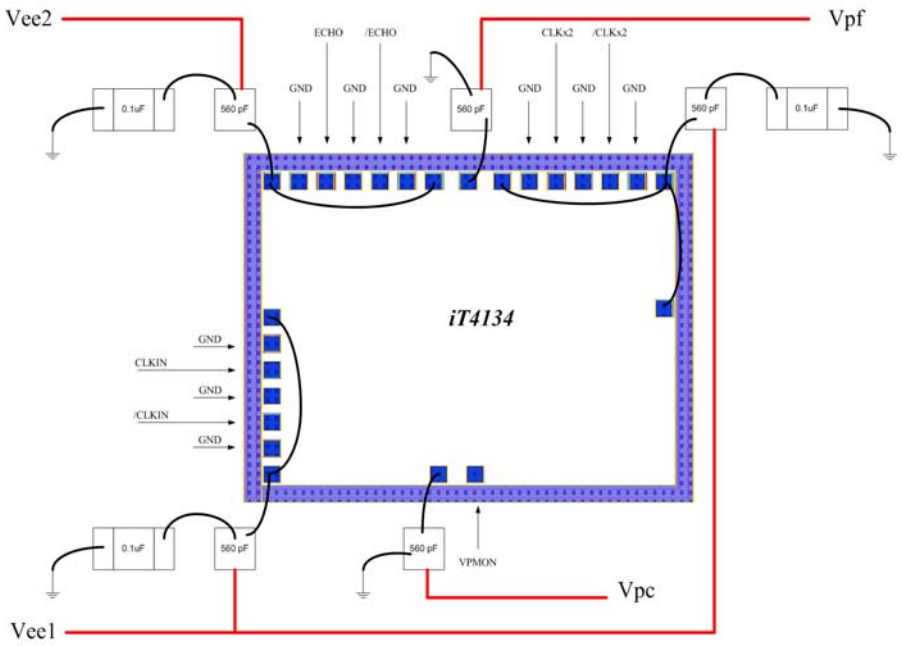
Recommended Mounting Assembly

Chip size
1900 µm ±10 mm
x 2400 µm ±10 µm
edge to edge

Chip thickness:
104 µm ±3 µm

Pad size:
100 µm x 100 µm

RF pad pitch:
150 µm



Pad Position and Chip Dimensions

Chip size
1900 µm ±10 mm
x 2400 µm ±10 µm
edge to edge

Chip thickness:
104 µm ±3 µm

Pad size:
100 µm x 100 µm

RF pad pitch:
150 µm